IN THE CLAIMS

1. (currently amended) A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a programming voltage to a first word line coupled to a control gate of the selected memory cell, wherein a gate/source voltage equal to the programming voltage is sufficient to cause a reversal of polarity of each memory cell;

applying a fraction of the programming voltage to other word lines coupled to control gates of non-selected memory cells not associated with the first word line;

applying a ground potential to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell; [[and]]

applying the fraction of the programming voltage to other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line and to other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line[[.]]; and

placing the selected memory cell in a normally-on state as a result of applying the programming voltage to the first word line and the ground potential to the first program line and the first bit line.

2. (original) The method of claim 1, wherein the programming voltage is approximately 6V.

3. (original) The method of claim 1, wherein the fraction of the programming voltage is approximately 1/2.

4. (currently amended) The method of claim 1, wherein a ~~gate/source~~ voltage across a ferroelectric layer of each memory cell equal to the fraction of the programming voltage is sufficient to cause a reversal of polarity of each memory cell.

5-19. (canceled)